AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A level transforming circuit comprising:

a first CMOS circuit which has first and second p-channel type MOS ~~transistor~~ transistors connected in series between a high voltage electricity source and a first output node, and first and second n-channel type MOS ~~transistor~~ transistors connected in series between said first output node and ~~the~~ ground, wherein a gate of said first p-channel type MOS transistor which functions ~~functioning~~ as a pull up switch is impressed with a first signal, wherein a gate of second n-channel type MOS transistor which functions ~~functioning~~ as a pull down switch is impressed with an input signal having an amplitude between a low voltage electricity source and the ground, and wherein gates of said second p-channel type MOS transistor and said first n-channel type MOS transistor are impressed with the low voltage electricity source ~~in common~~;

a first intermediate circuit which has a third p-channel type MOS transistor connected between the high voltage electricity source and a second output node, wherein a ~~its~~ gate of said third p-channel type MOS transistor is impressed with said first signal, and which has a third n-channel type MOS transistor connected between said second output node and the low voltage electricity source, wherein a ~~its~~ gate of said third n-channel type MOS transistor is impressed with said first signal;

a second intermediate circuit which has a fourth p-channel type MOS transistor connected between the high voltage electricity source and ~~the second~~ a third output node, wherein a ~~its~~ gate of said fourth p-channel type MOS transistor is impressed with electric potential of said second output node ~~of said first intermediate circuit~~, and which has a fourth n-channel type MOS

transistor connected between the third output node and the low voltage electricity source, wherein a ~~its~~ gate of said fourth n-channel type MOS transistor is impressed with the electric potential of said second output node, and which outputs ~~puts out~~ said first signal from said third output node;

a second CMOS circuit which has fifth and sixth p-channel type MOS ~~transistor~~ transistors connected in series between the high voltage electricity source and a fourth output node, and which has fifth and sixth n-channel type MOS ~~transistor~~ transistors connected in series between said fourth output node and the ground, wherein a gate of said fifth p-channel type MOS transistor which functions ~~functioning~~ as a pull up switch is impressed with the ~~a signal having~~ electric potential of said second output node ~~of first intermediate circuit~~, and wherein a gate of said sixth n-channel type MOS transistor which functions ~~functioning~~ as a pull down switch is impressed with an inverse signal of the input signal, and wherein gates of said sixth p-channel type MOS transistor and fifth n-channel type MOS transistor are impressed with the low voltage electricity source ~~in common~~, and wherein a signal having amplitude of said high voltage and ground voltage is output ~~put out~~ from said fourth output node;

a seventh p-channel type MOS transistor which is connected between a common node of said first and second p-channel type MOS transistors ~~in series~~ and said second output node, wherein a gate of said seventh p-channel type MOS transistor ~~N3 of said first intermediate circuit and which gate~~ is impressed with electric potential of said first output node of said first CMOS circuit;

an eighth p-channel type MOS transistor which is connected between a common node of said fifth and sixth p-channel type MOS transistors ~~in series~~ and said third output node, wherein a gate of said eighth p-channel type MOS transistor ~~of said second intermediate circuit and which gate~~ is impressed with electric potential of said fourth output node of said second CMOS circuit.

2. (Currently Amended) A level transforming circuit according to Claim 1[[:]], wherein:

a turn-on ~~turning on~~ resistance of said first p-channel type MOS transistor in said first CMOS circuit is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said second p-channel type MOS transistor, and a turn-on ~~turning on~~ resistance of said second n-channel type MOS transistor is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said first n-channel type MOS transistor;

a turn-on ~~turning on~~ resistance of said fifth p-channel type MOS transistor in said second CMOS circuit is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said sixth p-channel type MOS transistor, and a turn-on ~~turning on~~ resistance of said sixth n-channel type MOS transistor is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said fifth n-channel type MOS transistor;

a turn-on ~~turning on~~ resistance of said third p-channel type MOS transistor in said first intermediate circuit is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said seventh p-channel type MOS transistor; and

a turn-on ~~turning on~~ resistance of said fourth p-channel type MOS transistor in said second intermediate circuit is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said eighth p-channel type MOS transistor.

3. (Currently Amended) A level transforming circuit according to Claim 1[[:]], wherein:

a substrate of said third n-channel type MOS transistor in said first intermediate circuit is connected with a source of said third n-channel type MOS transistor, and a substrate of said fourth n-channel type MOS transistor in said second intermediate circuit is connected with a source of said fourth n-channel type MOS transistor; and

said substrate of said third n-channel type MOS transistor and said substrate of said fourth n-channel type MOS transistor are isolated from a substrate of each of said first, second, fifth and sixth n-channel type MOS transistors ~~transistor~~.

4. (Currently Amended) A level transforming circuit according to Claim 1[[:]], wherein:

a substrate ~~substrates~~ of each of said seventh p-channel type MOS transistor and ~~an~~ said eighth p-channel type MOS transistor is ~~are~~ connected to a respective ~~with each~~ source of each of said seventh and eighth p-channel type MOS transistors ~~or each drain~~; and

said substrate of said seventh p-channel type MOS transistor and said substrate of said eighth p-channel type MOS transistor are isolated from a substrate of each of said first to sixth n-channel type MOS ~~transistor~~ transistors.

5. (Currently Amended) A level transforming circuit according to Claim 1[[:]], wherein:

said first to eighth p-channel type MOS transistors and said first to sixth n-channel type MOS transistors ~~transistor~~ are formed on an active region isolated by insulating film.

6. (Currently Amended) A level transforming circuit according to Claim 1[[:]], wherein:

said first signal is a signal having an amplitude between the high voltage and the low voltage, and said first signal is output ~~put out~~ independently of said output signal.

7. (Currently Amended) A level transforming circuit comprising:

a first CMOS circuit which has first and second p-channel type MOS ~~transistor~~ transistors connected in series between a high voltage electricity source and a first output node, and first and second n-channel type MOS ~~transistor~~ transistors connected in series between said first output node and ~~the~~ ground, wherein a gate of said first p-channel type MOS transistor which functions ~~functioning~~ as a pull up switch is impressed with a first signal, wherein a gate of second n-channel type MOS transistor which functions ~~functioning~~ as a pull down switch is impressed with an input signal having an amplitude between a low voltage electricity source and the ground, and wherein gates of said second p-channel type MOS transistor and said first n-channel type MOS transistor are impressed with the low voltage electricity source ~~in common~~;

a first intermediate circuit which has a third p-channel type MOS transistor connected between the high voltage electricity source and a second output node, wherein a ~~its~~ gate of said third p-channel type MOS transistor is impressed with said first signal, and which has a third n-channel type MOS transistor connected between said second output node and the low voltage electricity source, wherein a ~~its~~ gate of said third n-channel type MOS transistor is impressed with said first signal;

a second intermediate circuit which has a fourth p-channel type MOS transistor connected between the high voltage electricity source and ~~the second~~ a third output node, wherein a ~~its~~ gate of said fourth p-channel type MOS transistor is impressed with electric potential of said second output node ~~of said first intermediate circuit~~, and which has a fourth n-channel type MOS transistor connected between the third output node and the low voltage electricity source, wherein a ~~its~~ gate of said fourth n-channel type MOS transistor is impressed with the electric potential of said second output node, and which outputs ~~puts out~~ said first signal from said third output node;

a second CMOS circuit which has fifth and sixth p-channel type MOS ~~transistor~~ transistors connected in series between the high voltage electricity source and a fourth output node, and which has fifth and sixth n-channel type MOS ~~transistor~~ transistors connected in series between said fourth output node and the ground, wherein a gate of said fifth p-channel type MOS transistor which functions ~~functioning~~ as a pull up switch is impressed with the ~~a signal having~~ electric potential of said second output node ~~of first intermediate circuit~~, and wherein a gate of said sixth n-channel type MOS transistor which functions ~~functioning~~ as a pull down switch is impressed with an inverse signal of the input signal, and wherein gates of said sixth p-channel type MOS transistor and fifth n-channel type MOS transistor are impressed with the low voltage electricity source ~~in common~~, and wherein a signal having amplitude of said high voltage and ground voltage is output ~~put out~~ from said fourth output node;

a seventh p-channel type MOS transistor which is connected between a common node of said first and second p-channel type MOS transistors ~~in series~~ and said second output node,

wherein a gate of said seventh p-channel type MOS transistor ~~of said first intermediate circuit and which gate~~ is impressed with electric potential of said low voltage;

an eighth p-channel type MOS transistor which is connected between a common node of said fifth and sixth p-channel type MOS transistors ~~in series~~ and said third output node, wherein a gate of said eighth p-channel type MOS transistor ~~of said second intermediate circuit and which gate~~ is impressed with electric potential of said low voltage.

8. (Currently Amended) A level transforming circuit according to Claim 7[[:]], wherein:

a turn-on ~~turning on~~ resistance of said first p-channel type MOS transistor in said first CMOS circuit is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said second p-channel type MOS transistor, and a turn-on ~~turning on~~ resistance of said second n-channel type MOS transistor is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said first n-channel type MOS transistor;

a turn-on ~~turning on~~ resistance of said fifth p-channel type MOS transistor in said second CMOS circuit is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said sixth p-channel type MOS transistor, and a turn-on ~~turning on~~ resistance of said sixth n-channel type MOS transistor is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said fifth n-channel type MOS transistor;

a turn-on ~~turning on~~ resistance of said third p-channel type MOS transistor in said first intermediate circuit is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said seventh p-channel type MOS transistor; and

a turn-on ~~turning on~~ resistance of said fourth p-channel type MOS transistor in said second intermediate circuit is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said eighth p-channel type MOS transistor.

9. (Currently Amended) A level transforming circuit according to Claim 7[[:]], wherein:

a substrate of said third n-channel type MOS transistor in said first intermediate circuit is connected with source of said third n-channel type MOS transistor, and a substrate of said fourth n-channel type MOS transistor in said second intermediate circuit is connected with a source of said fourth n-channel type MOS transistor; and

said substrate of said third n-channel type MOS transistor and said substrate of said fourth n-channel type MOS transistor are isolated from a substrate of each of said first, second, fifth and sixth n-channel type MOS transistors ~~transistor~~.

10. (Currently Amended) A level transforming circuit according to Claim 7[[:]], wherein:

a substrate ~~substrates~~ of each of said seventh p-channel type MOS transistor and ~~an~~ said eighth p-channel type MOS transistor is ~~are~~ connected to a respective ~~with each~~ source of each of said seventh and eighth p-channel type MOS transistors ~~or each drain~~; and

said substrate of said seventh p-channel type MOS transistor and said substrate of said eighth p-channel type MOS transistor are isolated from a substrate of each of said first to sixth n-channel type MOS ~~transistor~~ transistors.

11. (Currently Amended) A level transforming circuit according to Claim 7[[:]], wherein:

said first to eighth p-channel type MOS transistors and said first to sixth n-channel type MOS transistors ~~transistor~~ are formed on an active region isolated by insulating film.

12. (Currently Amended) A level transforming circuit according to Claim 7[[:]], wherein:

said first signal is a signal having an amplitude between the high voltage and the low voltage, and said first signal is output ~~put out~~ independently of said output signal.

13. (Currently Amended) A level transforming circuit comprising:

a first CMOS circuit which has first and second p-channel type MOS ~~transistor~~ transistors connected in series between a high voltage electricity source and a first output node, and first and second n-channel type MOS ~~transistor~~ transistors connected in series between said first output node and ~~the~~ ground, wherein a gate of said first p-channel type MOS transistor which functions ~~functioning~~ as a pull up switch is impressed with a first signal, wherein a gate of second n-channel type MOS transistor which functions ~~functioning~~ as a pull down switch is impressed with an input signal having an amplitude between a low voltage electricity source and the ground, and wherein gates of said second p-channel type MOS transistor and said first n-channel type MOS transistor are impressed with the low voltage electricity source ~~in common~~;

a first intermediate circuit which has a third p-channel type MOS transistor connected between the high voltage electricity source and second output node, wherein a ~~its~~ gate of said third p-channel type MOS transistor is impressed with said first signal, and which has third

n-channel type MOS transistor connected between said second output node and the low voltage electricity source, wherein a ~~its~~ gate of said third n-channel type MOS transistor is impressed with said first signal;

a second intermediate circuit which has a fourth p-channel type MOS transistor connected between the high voltage electricity source and ~~the second~~ a third output node, wherein a ~~its~~ gate of said fourth p-channel type MOS transistor is impressed with electric potential of second output node of said first intermediate circuit, and which has a fourth n-channel type MOS transistor connected between the third output node and the low voltage electricity source, wherein a ~~its~~ gate of said fourth n-channel type MOS transistor is impressed with the electric potential of said second output node, and which outputs ~~puts out~~ said first signal from said third output node;

a second CMOS circuit which has fifth and sixth p-channel type MOS ~~transistor~~ transistors connected in series between the high voltage electricity source and a fourth output node, and which has fifth and sixth n-channel type MOS ~~transistor~~ transistors connected in series between said fourth output node and the ground, wherein a gate of said fifth p-channel type MOS transistor which functions ~~functioning~~ as a pull up switch is impressed with the ~~a signal having~~ electric potential of said second output node ~~of first intermediate circuit~~, and wherein a gate of said sixth n-channel type MOS transistor which functions ~~functioning~~ as a pull down switch is impressed with an inverse signal of the input signal, and wherein gates of said sixth p-channel type MOS transistor and fifth n-channel type MOS transistor are impressed with the low voltage electricity source ~~in common~~, and wherein a signal having amplitude of said high voltage and ground voltage is output ~~put out~~ from said fourth output node;

a seventh n-channel type MOS transistor which is connected between a common node of said first and second p-channel type MOS transistors ~~in series~~ and said second output node, wherein a gate of said seventh n-channel type MOS transistor ~~of said first intermediate circuit and which gate~~ is impressed with electric potential of said high voltage;

an eighth n-channel type MOS transistor which is connected between a common node of said fifth and sixth p-channel type MOS transistors ~~in series~~ and said third output node, wherein a gate of said eighth n-channel type MOS transistor ~~of said second intermediate circuit and which gate~~ is impressed with electric potential of said high voltage.

14. (Currently Amended) A level transforming circuit according to Claim 13[[:]], wherein:

a turn-on ~~turning on~~ resistance of said first p-channel type MOS transistor in said first CMOS circuit is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said second p-channel type MOS transistor, and a turn-on ~~turning on~~ resistance of said second n-channel type MOS transistor is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said first n-channel type MOS transistor;

a turn-on ~~turning on~~ resistance of said fifth p-channel type MOS transistor in said second CMOS circuit is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said sixth p-channel type MOS transistor, and a turn-on ~~turning on~~ resistance of said sixth n-channel type MOS transistor is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said fifth n-channel type MOS transistor;

a turn-on ~~turning on~~ resistance of said third p-channel type MOS transistor in said first intermediate circuit is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said seventh n-channel type MOS transistor; and

a turn-on ~~turning on~~ resistance of said fourth p-channel type MOS transistor in said second intermediate circuit is ~~set~~ higher than a turn-on ~~turning on~~ resistance of said eighth n-channel type MOS transistor.

15. (Currently Amended) A level transforming circuit according to Claim 13[[:]], wherein:

a substrate of said third n-channel type MOS transistor in said first intermediate circuit is connected with a source of said third n-channel type MOS transistor, and a substrate of said fourth n-channel type MOS transistor in said second intermediate circuit is connected with a source of said fourth n-channel type MOS transistor; and

said substrate of said third n-channel type MOS transistor and said substrate of said fourth n-channel type MOS transistor are isolated from a substrate of each of said first, second, fifth and sixth n-channel type MOS transistors ~~transistor~~.

16. (Canceled)

17. (Currently Amended) A level transforming circuit according to Claim 13[[:]], wherein:

said first to sixth p-channel type MOS transistors and said first to eighth n-channel type MOS transistors ~~transistor~~ are formed on an active region isolated by insulating film.

18. (Currently Amended) A level transforming circuit according to Claim 13[[:]], wherein:

said first signal is a signal having an amplitude between the high voltage and the low voltage, and said first signal is output ~~put out~~ independently of said output signal.